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AXI®, PCIe®, and Ethernet or memory models for DRAM and Flash standards. Thu, 07 Feb 2019 08:20:00 GMT Mentor Verification IP - Mentor Graphics - arithmetic core lphaAdditional info:FPGA provenWishBone Compliant: NoLicense: LGPLDescriptionRTL Verilog code to perform Two Dimensional Fast Hartley Transform (2D-FHT) for 8x8 points.Presented algorithm is FHT with decimation in frequency domain.Main FeaturesHigh Clock SpeedLow Latency(97 clock cycles)Low Slice CountSingle Clock Cycle per ... Tue, 12 Feb 2019 14:48:00 GMT Free Range Factory - "The Dini Group is the future of FPGA Cluster Computing, High Performance Computing (HPC) and ASIC prototyping" Mon, 11 Feb 2019 13:59:00 GMT Dini Group - DNPCIe_40G_KU_LL_2Q SFP Kintex UltraScale, Low ... - A very warm welcome to my most ambitious project to date. In this project I'm going to attempt to design and build a sprite-based graphics accelerator that will function as a co-processor to an MCU. Fri, 15 Feb 2019 06:02:00 GMT An FPGA sprite graphics accelerator with a 180MHz ... - SYSMON User Guide 6 UG580 (v1.9) March 29, 2018 www.xilinx.com Chapter 1 Overview and

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